What is claimed is:

1. A high electron mobility transistor comprises:

a charge donor layer comprised of a first Group III-V material and a channel layer disposed adjacent said charge donor layer and comprised of a second Group III-V material having a bandgap energy lower than the bandgap energy of said first Group III-V material;

a pair of ohmic contacts disposed over first portions of said charge donor and channel layers and a Schottky barrier contact disposed over second portions of said charge donor and channel layers; and

means for shielding at least one of said charge donor and channel layers from the effects of surface charges which are present in regions between gate and drain electrodes of the transistor.

2. The structure, as recited in Claim 1, wherein said shielding means includes a portion of said charge donor layer with a first portion adjacent said channel being of an undoped Group III-V material a immediate portion adjacent said undoped portion comprised of a dopant sheet of N-type dopant having a concentration of dopant atoms confined to a few atomic layer thicknesses of the charge donor layer and a third portion of said layer being a relatively lightly doped region of said charge donor layer.

3. The transistor, as recited in Claim 1, wherein said shielding means comprises a pair of charge screen layers comprised of relatively lightly doped Group III-V materials disposed adjacent the gate electrode, and source and drain electrodes of the high electron mobility transistor.

4. The high electron mobility transistor, as recited in Claim 3, wherein said shielding means further comprises a recess having a first width disposed through the first charge screen layer and a second recess aligned over the first recess having a second, substantially larger width than that of the first recess disposed through a portion of the first charge screen layer and the second charge screen layer.

5. A high electron mobility transistor comprises:

a semi-insulating substrate;

a channel layer comprised of a first Group III-V material disposed over said semi-insulating substrate;

a charge donor region comprised of a first region of undoped Group III-V material having a bandgap higher than the corresponding bandgap of the channel layer, a region of said layer having a dopant profile confined to a few angstroms thickness of said layer and having a dopant concentration generally in the range of about $2.0X10^{12}$ to

$5X10^{12}$ atoms per square centimeter, said charge donor layer having a third region comprised of a relatively lightly doped portion of said second Group III-V material;

a charge screen layer comprised of a lightly doped N-type region of said first Group III-V material disposed over said third region of said charge donor layer;

a pair of spaced contact regions comprised of said first Group III-V material having a dopant concentration greater than about $1X10^{18}$ a/cc disposed over said charge screen layer;

a gate electrode disposed in Schottky barrier contact with said third portion of said charge donor layer; and

a pair of source and drain electrodes disposed in ohmic contact with said spaced contact layers.

6. The structure, as recited in Claim 5, wherein said gate electrode is disposed within a first aperture provided in said third portion of said charge donor layer and a selective portion of said charge screen layer and wherein said charge screen layer and spaced contact layer have a second relatively wide aperture compared to that of the first aperture disposed in alignment over the first aperture.

add A2